What is claimed is:

1. An addressing circuit for addressing a cross-point memory array having first and second sets of address lines, the addressing circuit comprising:

a first set of cross-point resistive elements connected to the first set of address lines;

a second set of cross-point resistive elements connected to the second set of address lines; and

at least one of a pull-up cross-point resistive element connected to the first set of address lines, and a pull-down cross-point resistive element connected to the second set of address lines.

2. The addressing circuit of claim 1, wherein each of the cross-point resistive elements of claim 1 share a same first conductive layer, a same second conductive layer, and a same semiconductor layer provided between the first conductive layer and the second conductive layer.

3. The addressing circuit of claim 1, wherein the cross-point memory array comprises a plurality of cross-point memory elements, each including a cross-point resistive element in series with a write-once circuit element, wherein one of the cross-point memory elements has an input connected to the pull-up cross-point resistive element and an output connected to the pull-down cross-point resistive element.

4. The addressing circuit of claim 3, wherein the first and second set of cross-point resistive elements, the pull-up and pull-down cross-point resistive elements, and the cross-point memory elements are formed in the same fabrication process.

5. The addressing circuit of claim 3, wherein the first and second set of cross-point resistive elements, the pull-up and pull-down cross-point resistive elements, and the cross-point resistive elements in the memory elements have substantially the same temperature coefficient of resistivity.

6. The addressing circuit of claim 3, wherein the first and second set of cross-point resistive elements, the pull-up and pull-down cross-point resistive elements, and the cross-point resistive elements in the memory elements are formed from substantially the same materials and include the same cross-point structure.

7. The addressing circuit of claim 3, wherein a resistance of at least one of the pull-up cross-point resistive element and the pull-down cross-point resistive element is approximately equal to Rlow * X, wherein Rlow is a resistance of the one of the cross-point memory elements in a low impedance state and X is a range between .1 and 10 inclusive.

8. The addressing circuit of claim 3, further comprising a first sense line operable to detect a binary state of the one of the cross-point memory elements, the first sense line

including a first sense line cross-point resistive element connected to the pull-up cross-point resistive element and the one of the cross-point memory elements.

9. The addressing circuit of claim 8, further comprising a second sense line operable to detect a binary state of the one of the cross-point memory elements, the second sense line including a second sense line cross-point resistive element connected to the pull-down cross-point resistive element and the one of the cross-point memory elements.

10. The addressing circuit of claim 9, wherein the first and second set of cross-point resistive elements, the pull-up and pull-down cross-point resistive elements, the cross-point resistive elements in the memory elements, the first sense line cross-point resistive element, and the second sense line cross-point resistive element include diodes.

11. The addressing circuit of claim 10, wherein anodes of the first set of cross-point resistive elements and the first sense line cross-point resistive element are connected to an output of the pull-up cross-point resistive element and cathodes of the second set of cross-point resistive elements and the second sense line cross-point resistive element are connected to an input of the pull-down cross-point resistive element.

12. A memory circuit comprising:

a cross-point memory array having first and second sets of transverse electrodes with respective memory elements formed at the crossing-points of the first and second set electrodes, each memory element including, a cross-point resistive element; and

an addressing circuit comprising:

a first set of cross-point resistive elements connected between the first set of address lines and the first set of memory array electrodes;

a second set of cross-point resistive elements connected between the second set of address lines and the second set of memory array electrodes;

a set of pull-up cross-point resistive elements connected to the first set of address lines and first set of transverse electrodes; and

a set of pull-down cross-point resistive elements connected to the second set of address lines and the second set of transverse electrodes.

13. The memory circuit of claim 12, wherein the addressing circuit further comprises at least one sense line including a sense line cross-point resistive element connected to at least one of the first set of transverse electrodes and the second set of transverse electrodes.

14. The memory circuit of claim 13, wherein the cross-point resistive elements for each memory element, the first set of cross-point resistive elements, the second set of cross-point resistive elements, the set of pull-up and the set of pull-down cross-point resistive elements, and the sense line cross-point resistive element each share a same first conductive layer, a same second conductive layer, and substantially a same semiconductor layer provided between the first conductive layer and the second conductive layer.

15. The memory circuit of claim 13, wherein the cross-point resistive elements for each memory element, the first set of cross-point resistive elements, the second set of cross-point resistive elements, the set of pull-up and the set of pull-down cross-point resistive elements, and the sense line cross-point resistive element each are formed in the same fabrication process.

16. The memory circuit of claim 13, wherein the cross-point resistive elements for each memory element, the first set of cross-point resistive elements, the second set of cross-point resistive elements, the set of pull-up and the set of pull-down cross-point resistive elements, and the sense line cross-point resistive element have substantially the same temperature coefficient of resistivity.

17. The addressing circuit of claim 13, wherein a resistance of each of the set of pull-up and the set of pull-down cross-point resistive elements is approximately equal to Rlow * X, wherein Rlow is a resistance of a cross-point resistive element included with one of the memory elements in a low impedance state and X is a range between .1 and 10 inclusive.

18. The memory circuit of claim 13, wherein the cross-point resistive elements for each memory element, the first set of cross-point resistive elements, the second set of cross-point resistive elements, the set of pull-up and the set of pull-down cross-point resistive elements, and the sense line cross-point resistive element each comprises a diode.

19. The memory circuit of claim 12, further comprising a plurality of stacked integrated circuits, each integrated circuit including the memory circuit of claim 12 and being addressable in parallel to read or write data from one or more of the plurality of stacked integrated circuits.

20. A method for determining the state of a memory element of a plurality of memory elements in a cross-point memory array, the method comprising:

addressing the memory element by applying predetermined electrical signals to a first set of address lines including a first set of cross-point resistive elements connected to the memory element and by applying predetermined electrical signals to a second set of address lines including a second set of cross-point resistive elements connected to the memory element;

generating a current using at least one of a pull-up cross-point resistive element connected to the first set of address lines and a pull-down cross-point resistive element connected to the second set of address lines; and

sensing a binary state of the memory element based on the generated current and using at least one sense line connected to at least one of the pull-up cross-point resistive element and the pull-down cross-point resistive element and further connected to the memory element.

21. The method of claim 20, further comprising applying a predetermined electrical signal to the at least one sense line for enabling or preventing writing to the addressed memory element.

22. The method of claim 20, wherein the at least one sense line includes a sense line cross-point resistive element.

23. The method of claim 22, wherein the memory element, the first set of cross-point resistive elements, the second set of cross-point resistive elements, the pull-up and pull-down cross-point resistive elements, and the sense line cross-point resistive element have the same cross-point structure and are formed using substantially the same materials.

24. The method of claim 20, wherein a resistance of at least one of the pull-up cross-point resistive element and the pull-down cross-point resistive element is approximately equal to Rlow * X, wherein Rlow is a resistance of the memory elements in a low impedance state and X is a range between .1 and 10 inclusive.

25. An apparatus including a memory array having at least one memory element, the apparatus comprising:

means for addressing a memory element in the memory array by applying predetermined electrical signals to a first set of address lines including a first set of cross-point resistive elements connected to the memory element and by applying predetermined electrical signals to a second set of address lines including a second set of cross-point resistive elements connected to the memory element;

means for generating a current using at least one of a pull-up cross-point resistive element connected to the first set of address lines and a pull-down cross-point resistive element connected to the second set of address lines; and

means for sensing a binary state of the memory element based on the generated current and using at least one sense line connected to at least one of the pull-up cross-point resistive element and the pull-down cross-point resistive element and further connected to the memory element.

26. The apparatus of claim 25, further comprising means for applying a predetermined electrical signal to the at least one sense line for enabling or preventing writing to the addressed memory element.

27. The apparatus of claim 25, wherein the at least one sense line includes a sense line cross-point resistive element.

28. The apparatus of claim 27, wherein the memory element, the first set of cross-point resistive elements, the second set of cross-point resistive elements, the pull-up and pull-down cross-point resistive elements, and the sense line cross-point resistive element have the same cross-point structure and are formed using substantially the same materials.

29. The apparatus of claim 25, wherein a resistance of at least one of the pull-up cross-point resistive element and the pull-down cross-point resistive element is approximately equal to Rlow * X, wherein Rlow is a resistance of the memory elements in a low impedance state and X is a range between .1 and 10 inclusive.